REMARKS/ARGUMENTS

Claims 2-12 and 14-20 are currently pending in the present patent application, with claims 1 and 13 having been cancelled through the above claim amendments.

In an Office Action mailed on October 18, 2005, the Examiner allowed claims 8-12, objected to claims 3, 14, and 17-20, and rejected claims 1, 2, 4-7, 14, 15-18, and 20 as being anticipated by U.S. Patent No. 6,212,670 to Kaviani ("Kaviani"). Claims 17-20 were objected to for several minor informalities and the claims have been amended to eliminate these informalities. These amendments do not narrow the scopes of any of these claims. Claims 4 and 7 were also rejected under the second paragraph of 35 U.S.C. § 112 and have been amended to eliminate any deficiencies under this section. Once again, these amendments do not narrow the scopes of these claims. Claims 3 and 14 have been rewritten in independent form and are now allowable along with claims 2, 4-6, and 15 that depend from these claims.

Amended independent claim 7 recites an improved system for mapping an electronic digital circuit to a Look up table (LUT) based Programmable Logic Device (PLD). The method includes selecting means for selecting an unmapped or partially mapped LUT and grouping means for clustering circuit elements for mapping based on an available capacity of the selected LUT and at least one mapping constraint. Mapping means map the group of circuit elements onto the selected LUT. The grouping means and mapping means include the mapping of cascade logic associated with the selected LUT after mapping of the group of circuit elements onto the LUT.

Kaviani neither discloses nor suggests the method recited in amended claim 7. As shown in Figure 6 of Kaviani, logic for being implemented in LUTs and as PLA blocks is performed in step 106. There is no disclosure nor suggestion of the mapping of cascade logic associated with the selected LUT after mapping of the group of circuit elements onto the LUT. This is acknowledged by the Examiner in paragraph 8 of the Office Action. For these reason, the combination of elements recited in amended claim 7 is allowable.

Amended claim 16 recites, in part, an electronic system for programming a programmable logic device. The programmable logic device includes look-up tables and cascade elements, and the electronic system includes a mapping circuit coupled to a selection and a logic grouping circuit. The mapping circuit is operable to map grouped

logic into the selected look-up table and into the cascade elements as a function of the available capacity of the selected look-up table. The mapping circuit maps the cascade logic after the grouped logic is mapped into the selected look-up table. Once again, Kaviani neither discloses nor suggests mapping cascade logic after mapping the logic into the LUT, as recited in amended claim 16.

For these reasons, the combination of elements recited in claim 16 is allowable. Dependent claims 17-20 are allowable for at least the same reasons as claim 16 and due to the additional limitations added by each of these claims.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. Should the Examiner have any further questions about the application, Applicant respectfully requests the Examiner to contact the undersigned attorney at (425) 455-5575 to resolve the matter. If any need for any fee in addition to that paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

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